PIN	Type	Function	i.MX6 Dual Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
3rd UART						
67	3V3	TXD	EIM_D24	EIM_DATA24 ECSPI4_SS2 UART3_TX_DATA ECSPI1_SS2 ECSPI2_SS2 AUD5_RXFS UART1_DTR_B EPDC_SDCE7	GPIO3[24]	Application UART 3 Transmit Data output signal
68	3V3	RXD	EIM_D25	EIM_DATA25 ECSPI4_SS3 UART3_RX_DATA ECSPI1_SS3 ECSPI2_SS3 AUD5_RXC UART1_DSR_B EPDC_SDCE8	GPIO3[25]	Application UART 3 Receive Data input signal
69	3V3	RTS	SD3_RST	SD3_RESET UART3_RTS_B	GPIO7[8]	Application UART 3 Request to Send **input** signal
70	3V3	CTS	SD3_DAT3	SD3_DATA3 UART3_CTS_B	GPIO7[7]	Application UART 3 Clear to Send **output** signal
71	GND	GND				
KEYPAD / 1st CAN						
72	3V3	KP_COL[0]	GPIO_9	ESAI_RX_FS WDOG1_B KEY_COL6 CCM_REF_EN_B PWM1_OUT SD1_WP	GPIO1[9]	
73	3V3	KP_COL[1]	GPIO_4	ESAI_TX_HF_CLK KEY_COL7 SD2_CD_B	GPIO1[4]	
74	3V3	KP_COL[2]	KEY_COL2	ECSPI1_SS1 ENET_RX_DATA2 FLEXCAN1_TX KEY_COL2 ENET_MDC USB_H1_PWR_CTL_WAKE	GPIO4[10]	
75	3V3	KP_COL[3]	KEY_COL3	ECSPI1_SS3 ENET_CRS HDMI_TX_DDC_SCL KEY_COL3 I2C2_SCL SPDIF_IN	GPIO4[12]	
76	3V3	TXCAN	KEY_COL4	FLEXCAN2_TX IPU1_SISG4 USB_OTG_OC KEY_COL4 UART5_RTS_B	GPIO4[14]	
77	3V3	KP_ROW[0]	GPIO_2	ESAI_TX_FS KEY_ROW6 SD2_WP MLB_DATA	GPIO1[2]	
78	3V3	KP_ROW[1]	GPIO_5	ESAI_TX2_RX3 KEY_ROW7 CCM_CLKO1 I2C3_SCL ARM_EVENTI	GPIO1[5]	
79	3V3	KP_ROW[2]	KEY_ROW2	ECSPI1_SS2 ENET_TX_DATA2 FLEXCAN1_RX KEY_ROW2 SD2_VSELECT HDMI_TX_CEC_LINE	GPIO4[11]	
80	3V3	KP_ROW[3]	KEY_ROW3	ASRC_EXT_CLK HDMI_TX_DDC_SDA KEY_ROW3 I2C2_SDA SD1_VSELECT	GPIO4[13]	
81	3V3	RXCAN	KEY_ROW4	FLEXCAN2_RX IPU1_SISG5 USB_OTG_PWR KEY_ROW4 UART5_CTS_B	GPIO4[15]	
82	GND	GND				

PIN	Type	Function	i.MX6 Dual Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
SSI 1 - Serial Audio Port 1						
83	3V3	SSI1_INT	EIM_D26	EIM_DATA26 IPU1_DI1_PIN11 IPU1_CSI0_DATA01 IPU1_CSI1_DATA14 UART2_TX_DATA IPU1_SISG2 IPU1_DISP1_DATA22 EPDC_SDOED	**GPIO3[26]**	GPIO
84	3V3	SSI1_RXD	KEY_ROW1	ECSPI1_SS0 ENET_COL AUD5_RXD KEY_ROW1 UART5_RX_DATA SD2_VSELECT	GPIO4[9]	Serial Audio Interface serial data line 1
85	3V3	SSI1_TXD	KEY_ROW0	ECSPI1_MOSI ENET_TX_DATA3 AUD5_TXD KEY_ROW0 UART4_RX_DATA DCIC2_OUT	GPIO4[7]	Serial Audio Interface serial data line 0
86	3V3	SSI1_CLK	KEY_COL0	ECSPI1_SCLK ENET_RX_DATA3 AUD5_TXC KEY_COL0 UART4_TX_DATA DCIC1_OUT	GPIO4[6]	Serial Audio Interface serial bit clock
87	3V3	SSI1_FS	KEY_COL1	ECSPI1_MISO ENET_MDIO AUD5_TXFS KEY_COL1 UART5_TX_DATA SD1_VSELECT	GPIO4[8]	Serial Audio Interface left/right clock
88	GND	GND				
SSI 2 - Serial Audio Port 2						
89	3V3	SSI2_INT	EIM_D27	EIM_DATA27 IPU1_DI1_PIN13 IPU1_CSI0_DATA00 IPU1_CSI1_DATA13 UART2_RX_DATA IPU1_SISG3 IPU1_DISP1_DATA23 EPDC_SDOE	**GPIO3[27]**	GPIO
90	3V3	SSI2_RXD	CSI0_DAT7	IPU1_CSI0_DATA07 EIM_DATA05 ECSPI1_SS0 KEY_ROW6 AUD3_RXD ARM_TRACE04	GPIO5[25]	Serial Audio Interface serial data line 1
91	3V3	SSI2_TXD	CSI0_DAT5	IPU1_CSI0_DATA05 EIM_DATA03 ECSPI1_MOSI KEY_ROW5 AUD3_TXD ARM_TRACE02	GPIO5[23]	Serial Audio Interface serial data line 0
92	3V3	SSI2_CLK	CSI0_DAT4	IPU1_CSI0_DATA04 EIM_DATA02 ECSPI1_SCLK KEY_COL5 AUD3_TXC ARM_TRACE01	GPIO5[22]	Serial Audio Interface serial bit clock
93	3V3	SSI2_FS	CSI0_DAT6	IPU1_CSI0_DATA06 EIM_DATA04 ECSPI1_MISO KEY_COL6 AUD3_TXFS ARM_TRACE03	GPIO5[24]	Serial Audio Interface left/right clock
94	GND	GND				

PIN	Type	Function	i.MX6 Dual Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
Secure Digital Interface 2						
95	3V3	SD2_CD	SD3_CLK	SD3_CLK UART2_RTS_B FLEXCAN1_RX	GPIO7[3]	SD Card Detect – connected to a GPIO
96	3V3	SD2_D[0]	SD2_DAT0	SD2_DATA0 AUD4_RXD KEY_ROW7 / DCIC2_OUT	GPIO1[15]	SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50 K–69 K external pull up resistor must be added.
97	3V3	SD2_D[1]	SD2_DAT1	SD2_DATA1 EIM_CS2 AUD4_TXFS / KEY_COL7	GPIO1[14]	
98	3V3	SD2_D[2]	SD2_DAT2	SD2_DATA2 EIM_CS3 AUD4_TXD KEY_ROW6	GPIO1[13]	
99	3V3	SD2_D[3]	SD2_DAT3	SD2_DATA3 KEY_COL6 AUD4_TXC	GPIO1[12]	
100	3V3	SD2_CMD	SD2_CMD	SD2_CMD KEY_ROW5 AUD4_RXC	GPIO1[11]	SD Command bidirectional signal
101	3V3	SD2_CLK	SD2_CLK	SD2_CLK KEY_COL5 AUD4_RXFS	GPIO1[10]	SD Output Clock.
102	GND	GND				
CMOS Sensor Interface						
103	3V3	CSI0_DAT12	CSI0_DAT12	IPU1_CSI0_DATA12 EIM_DATA08 UART4_TX_DATA ARM_TRACE09	GPIO5[30]	
104	3V3	CSI0_DAT13	CSI0_DAT13	IPU1_CSI0_DATA13 EIM_DATA09 UART4_RX_DATA ARM_TRACE10	GPIO5[31]	
105	3V3	CSI0_DAT14	CSI0_DAT14	IPU1_CSI0_DATA14 EIM_DATA10 UART5_TX_DATA ARM_TRACE11	GPIO6[0]	
106	3V3	CSI0_DAT15	CSI0_DAT15	IPU1_CSI0_DATA15 EIM_DATA11 UART5_RX_DATA ARM_TRACE12	GPIO6[1]	
107	3V3	CSI0_DAT16	CSI0_DAT16	IPU1_CSI0_DATA16 EIM_DATA12 UART4_RTS_B ARM_TRACE13	GPIO6[2]	
108	3V3	CSI0_DAT17	CSI0_DAT17	IPU1_CSI0_DATA17 EIM_DATA13 UART4_CTS_B ARM_TRACE14	GPIO6[3]	
109	3V3	CSI0_DAT18	CSI0_DAT18	IPU1_CSI0_DATA18 EIM_DATA14 UART5_RTS_B ARM_TRACE15	GPIO6[4]	
110	3V3	CSI0_DAT19	CSI0_DAT19	IPU1_CSI0_DATA19 EIM_DATA15 UART5_CTS_B	GPIO6[5]	
111	GND	GND				
112	3V3	CSI0_HSYNC	CSI0_MCLK	IPU1_CSI0_HSYNC CCM_CLKO1 ARM_TRACE_CTL	GPIO5[19]	
113	3V3	CSI0_VSYNC	CSI0_VSYNC	IPU1_CSI0_VSYNC EIM_DATA01 ARM_TRACE00	GPIO5[21]	
114	3V3	CSI0_PIXCLK	CSI0_PIXCLK	IPU1_CSI0_PIXCLK ARM_EVENTO	GPIO5[18]	
115	3V3	CSI0_MCLK	GPIO_0	CCM_CLKO1 KEY_COL5 ASRC_EXT_CLK EPIT1_OUT USB_H1_PWR SNVS_VIO_5	GPIO1[0]	
116	GND	GND				

PIN	Type	Function	i.MX6 Dual Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
LCD Controller and Smart LCD Controller						
117	3V3	LD0	**DISP0_DAT0**	IPU1_DISP0_DATA00 LCD_DATA00 ECSPI3_SCLK	GPIO4[21]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS1_TX2_N	not available		TX6DL LVDS version: LVDS display output port 1
118	3V3	LD1	**DISP0_DAT1**	IPU1_DISP0_DATA01 LCD_DATA01 ECSPI3_MOSI	GPIO4[22]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS1_TX1_N	not available		TX6DL LVDS version: LVDS display output port 1
119	3V3	LD2	**DISP0_DAT2**	IPU1_DISP0_DATA02 LCD_DATA02 ECSPI3_MISO	GPIO4[23]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS1_TX2_P	not available		TX6DL LVDS version: LVDS display output port 1
120	3V3	LD3	**DISP0_DAT3**	IPU1_DISP0_DATA03 LCD_DATA03 ECSPI3_SS0	GPIO4[24]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS1_TX1_P	not available		TX6DL LVDS version: LVDS display output port 1
121	3V3	LD4	**DISP0_DAT4**	IPU1_DISP0_DATA04 LCD_DATA04 ECSPI3_SS1	GPIO4[25]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS1_TX3_N	not available		TX6DL LVDS version: LVDS display output port 1
122	3V3	LD5	**DISP0_DAT5**	IPU1_DISP0_DATA05 LCD_DATA05 ECSPI3_SS2 AUD6_RXFS	GPIO4[26]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS1_TX0_N	not available		TX6DL LVDS version: LVDS display output port 1
123	3V3	LD6	**DISP0_DAT6**	IPU1_DISP0_DATA06 LCD_DATA06 ECSPI3_SS3 AUD6_RXC	GPIO4[27]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS1_TX3_P	not available		TX6DL LVDS version: LVDS display output port 1
124	3V3	LD7	**DISP0_DAT7**	IPU1_DISP0_DATA07 LCD_DATA07 ECSPI3_RDY	GPIO4[28]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS1_TX0_P	not available		TX6DL LVDS version: LVDS display output port 1
125	3V3	LD8	**DISP0_DAT8**	IPU1_DISP0_DATA08 LCD_DATA08 PWM1_OUT WDOG1_B	GPIO4[29]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS1_CLK_N	not available		TX6DL LVDS version: LVDS display output port 1
126	3V3	LD9	**DISP0_DAT9**	IPU1_DISP0_DATA09 LCD_DATA09 PWM2_OUT WDOG2_B	GPIO4[30]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS0_TX3_P	not available		TX6DL LVDS version: LVDS display output port 0
127	3V3	LD10	**DISP0_DAT10**	IPU1_DISP0_DATA10 LCD_DATA10	GPIO4[31]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS1_CLK_P	not available		TX6DL LVDS version: LVDS display output port 1
128	3V3	LD11	**DISP0_DAT11**	IPU1_DISP0_DATA11 LCD_DATA11	GPIO5[5]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS0_TX3_N	not available		TX6DL LVDS version: LVDS display output port 0
129	GND	GND				
130	3V3	LD12	**DISP0_DAT12**	IPU1_DISP0_DATA12 LCD_DATA12	GPIO5[6]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS0_CLK_P	not available		TX6DL LVDS version: LVDS display output port 0
131	3V3	LD13	**DISP0_DAT13**	IPU1_DISP0_DATA13 LCD_DATA13 AUD5_RXFS	GPIO5[7]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS0_TX2_P	not available		TX6DL LVDS version: LVDS display output port 0

PIN	Type	Function	i.MX6 Dual Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
132	3V3	LD14	**DISP0_DAT14**	IPU1_DISP0_DATA14 LCD_DATA14 AUD5_RXC	GPIO5[8]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS0_CLK_N	not available		TX6DL LVDS version: LVDS display output port 0
133	3V3	LD15	**DISP0_DAT15**	IPU1_DISP0_DATA15 LCD_DATA15 ECSPI1_SS1 ECSPI2_SS1	GPIO5[9]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS0_TX2_N	not available		TX6DL LVDS version: LVDS display output port 0
134	3V3	LD16	**DISP0_DAT16**	IPU1_DISP0_DATA16 LCD_DATA16 ECSPI2_MOSI AUD5_TXC SDMA_EXT_EVENT0	GPIO5[10]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS0_TX1_P	not available		TX6DL LVDS version: LVDS display output port 0
135	3V3	LD17	**DISP0_DAT17**	IPU1_DISP0_DATA17 LCD_DATA17 ECSPI2_MISO AUD5_TXD SDMA_EXT_EVENT1	GPIO5[11]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS0_TX0_P	not available		TX6DL LVDS version: LVDS display output port 0
136	3V3	LD18	**DISP0_DAT18**	IPU1_DISP0_DATA18 LCD_DATA18 ECSPI2_SS0 AUD5_TXFS / AUD4_RXFS EIM_CS2	GPIO5[12]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS0_TX1_N	not available		TX6DL LVDS version: LVDS display output port 0
137	3V3	LD19	**DISP0_DAT19**	IPU1_DISP0_DATA19 LCD_DATA19 ECSPI2_SCLK AUD5_RXD / AUD4_RXC EIM_CS3	GPIO5[13]	TX6DL standard version: LCD Data Bus
	LVDS		LVDS0_TX0_N	not available		TX6DL LVDS version: LVDS display output port 0
138	3V3	LD20	**DISP0_DAT20**	IPU1_DISP0_DATA20 LCD_DATA20 ECSPI1_SCLK AUD4_TXC	GPIO5[14]	TX6DL standard version: LCD Data Bus
	SATA			not available		TX6DL LVDS version: not available
139	3V3	LD21	**DISP0_DAT21**	IPU1_DISP0_DATA21 LCD_DATA21 ECSPI1_MOSI AUD4_TXD	GPIO5[15]	TX6DL standard version: LCD Data Bus
	SATA			not available		TX6DL LVDS version: not available
140	3V3	LD22	**DISP0_DAT22**	IPU1_DISP0_DATA22 LCD_DATA22 ECSPI1_MISO AUD4_TXFS	GPIO5[16]	TX6DL standard version: LCD Data Bus
	SATA			not available		TX6DL LVDS version: not available
141	3V3	LD23	**DISP0_DAT23**	IPU1_DISP0_DATA23 LCD_DATA23 ECSPI1_SS0 AUD4_RXD	GPIO5[17]	TX6DL standard version: LCD Data Bus
	SATA			not available		TX6DL LVDS version: not available
142	GND	GND				
143	3V3	HSYNC	DI0_PIN2	IPU1_DI0_PIN02 LCD_HSYNC AUD6_TXD / LCD_RS	GPIO4[18]	
144	3V3	VSYNC	DI0_PIN3	IPU1_DI0_PIN03 LCD_VSYNC AUD6_TXFS LCD_CS	GPIO4[19]	
145	3V3	OE_ACD	DI0_PIN15	IPU1_DI0_PIN15 LCD_ENABLE AUD6_TXC LCD_RD_E	GPIO4[17]	
146	3V3	LSCLK	DI0_DISP_CLK	IPU1_DI0_DISP_CLK LCD_CLK LCD_WR_RWN	GPIO4[16]	
147	GND	GND				

PIN	Type	Function	i.MX6 Dual Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
Module Specific Signals						
148	3V3	CSI1_MCLK	NANDF_CS2	NAND_CE2_B IPU1_SISG0 ESAI_TX0 EIM_CRE CCM_CLKO2	GPIO6[15]	
149	3V3	CSI1_PIXCLK	EIM_A16	EIM_ADDR16 IPU1_DI1_DISP_CLK IPU1_CSI1_PIXCLK SRC_BOOT_CFG16 EPDC_DATA00	GPIO2[22]	
150	3V3	CSI1_VSYNC	EIM_D29	EIM_DATA29 IPU1_DI1_PIN15 ECSPI4_SS0 UART2_RTS_B IPU1_CSI1_VSYNC IPU1_DI0_PIN14 EPDC_PWR_WAKE	GPIO3[29]	
151	3V3	CSI1_HSYNC	EIM_EB3	EIM_EB3 ECSPI4_RDY UART3_RTS_B UART1_RI_B IPU1_CSI1_HSYNC IPU1_DI1_PIN03 SRC_BOOT_CFG31 EPDC_SDCE0 EIM_ACLK_FREERUN	GPIO2[31]	
152	3V3	CSI1_D[12]	EIM_A17	EIM_ADDR17 IPU1_DISP1_DATA12 IPU1_CSI1_DATA12 SRC_BOOT_CFG17 EPDC_PWR_STAT	GPIO2[21]	
153	3V3	CSI1_D[13]	EIM_A18	EIM_ADDR18 IPU1_DISP1_DATA13 IPU1_CSI1_DATA13 SRC_BOOT_CFG18 EPDC_PWR_CTRL0	GPIO2[20]	
154	3V3	CSI1_D[14]	EIM_A19	EIM_ADDR19 IPU1_DISP1_DATA14 IPU1_CSI1_DATA14 SRC_BOOT_CFG19 EPDC_PWR_CTRL1	GPIO2[19]	
155	3V3	CSI1_D[15]	EIM_A20	EIM_ADDR20 IPU1_DISP1_DATA15 IPU1_CSI1_DATA15 SRC_BOOT_CFG20 EPDC_PWR_CTRL2	GPIO2[18]	
156	3V3	CSI1_D[16]	EIM_A21	EIM_ADDR21 IPU1_DISP1_DATA16 IPU1_CSI1_DATA16 SRC_BOOT_CFG21 EPDC_GDCLK	GPIO2[17]	
157	3V3	CSI1_D[17]	EIM_A22	EIM_ADDR22 IPU1_DISP1_DATA17 IPU1_CSI1_DATA17 SRC_BOOT_CFG22 EPDC_GDSP	GPIO2[16]	
158	3V3	CSI1_D[18]	EIM_A23	EIM_ADDR23 IPU1_DISP1_DATA18 IPU1_CSI1_DATA18 IPU1_SISG3 SRC_BOOT_CFG23 EPDC_GDOE	GPIO6[6]	
159	3V3	CSI1_D[19]	EIM_A24	EIM_ADDR24 IPU1_DISP1_DATA19 IPU1_CSI1_DATA19 IPU1_SISG2 SRC_BOOT_CFG24 EPDC_GDRL	GPIO5[4]	
160	GND	GND				
161	3V3		CSI0_DAT8	IPU1_CSI0_DATA08 EIM_DATA06 ECSPI2_SCLK KEY_COL7 I2C1_SDA ARM_TRACE05	GPIO5[26]	

PIN	Type	Function	i.MX6 Dual Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
162	3V3		CSI0_DAT9	IPU1_CSI0_DATA09 EIM_DATA07 ECSPI2_MOSI KEY_ROW7 I2C1_SCL ARM_TRACE06	GPIO5[27]	
163	3V3		CSI0_DAT10	IPU1_CSI0_DATA10 AUD3_RXC ECSPI2_MISO UART1_TX_DATA ARM_TRACE07	GPIO5[28]	
164	3V3		CSI0_DAT11	IPU1_CSI0_DATA11 AUD3_RXFS ECSPI2_SS0 UART1_RX_DATA ARM_TRACE08	GPIO5[29]	
165	3V3		EIM_D22	EIM_DATA22 ECSPI4_MISO IPU1_DI0_PIN01 IPU1_CSI1_DATA10 USB_OTG_PWR SPDIF_OUT EPDC_SDCE6	GPIO3[22]	
166	LVDS		CLK1_N			Alternate reference clock for PCIe
167	LVDS		PCIE_RXM			
168	LVDS		CLK1_P			Alternate reference clock for PCIe
169	LVDS		PCIE_RXP			
170	LVDS		PCIE_TXM			
171	GND	GND				
172	LVDS		PCIE_TXP			
173	3V3	EIM_CS0	EIM_CS0	EIM_CS0 IPU1_DI1_PIN05 ECSPI2_SCLK EPDC_DATA06	GPIO2[23]	
174	3V3	EIM_CS1	EIM_CS1	EIM_CS1 IPU1_DI1_PIN06 ECSPI2_MOSI EPDC_DATA08	GPIO2[24]	
175	3V3	GPIO	CSI0_DATA_EN	IPU1_CSI0_DATA_EN EIM_DATA00 ARM_TRACE_CLK	GPIO5[20]	
176	3V3	EIM_WAIT	EIM_WAIT	EIM_WAIT EIM_DTACK_B SRC_BOOT_CFG25	GPIO5[0]	
177	3V3	EIM_EB0	EIM_EB0	EIM_EB0 IPU1_DISP1_DATA11 IPU1_CSI1_DATA11 CCM_PMIC_READY SRC_BOOT_CFG27 EPDC_PWR_COM	GPIO2[28]	
178	3V3	EIM_EB1	EIM_EB1	EIM_EB1 IPU1_DISP1_DATA10 IPU1_CSI1_DATA10 SRC_BOOT_CFG28 EPDC_SDSHR	GPIO2[29]	
179	3V3	EIM_OE	EIM_OE	EIM_OE IPU1_DI1_PIN07 ECSPI2_MISO EPDC_PWR_IRQ	GPIO2[25]	
180	3V3	EIM_LBA	EIM_LBA	EIM_LBA IPU1_DI1_PIN17 ECSPI2_SS1 SRC_BOOT_CFG26 EPDC_DATA04	GPIO2[27]	
181	3V3	EIM_RW	EIM_RW	EIM_RW IPU1_DI1_PIN08 ECSPI2_SS0 SRC_BOOT_CFG29 EPDC_DATA07	GPIO2[26]	
182	3V3	EIM_BCLK	EIM_BCLK	EIM_BCLK IPU1_DI1_PIN16 EPDC_SDCE9	GPIO6[31]	
183	GND	GND				

PIN	Type	Function	i.MX6 Dual Pad Name	Alternate functions	GPIO	Description (refer to i.MX6 Dual manuals for details)
184	3V3	EIM_DA0	EIM_DA0	EIM_AD00 IPU1_DISP1_DATA09 IPU1_CSI1_DATA09 SRC_BOOT_CFG00 EPDC_SDCLK_N	GPIO3[0]	
185	3V3	EIM_DA1	EIM_DA1	EIM_AD01 IPU1_DISP1_DATA08 IPU1_CSI1_DATA08 SRC_BOOT_CFG01 EPDC_SDLE	GPIO3[1]	
186	3V3	EIM_DA2	EIM_DA2	EIM_AD02 IPU1_DISP1_DATA07 IPU1_CSI1_DATA07 SRC_BOOT_CFG02 EPDC_BDR0	GPIO3[2]	
187	3V3	EIM_DA3	EIM_DA3	EIM_AD03 IPU1_DISP1_DATA06 IPU1_CSI1_DATA06 SRC_BOOT_CFG03 EPDC_BDR1	GPIO3[3]	
188	3V3	EIM_DA4	EIM_DA4	EIM_AD04 IPU1_DISP1_DATA05 IPU1_CSI1_DATA05 SRC_BOOT_CFG04 EPDC_SDCE0	GPIO3[4]	
189	3V3	EIM_DA5	EIM_DA5	EIM_AD05 IPU1_DISP1_DATA04 IPU1_CSI1_DATA04 SRC_BOOT_CFG05 EPDC_SDCE1	GPIO3[5]	
190	3V3	EIM_DA6	EIM_DA6	EIM_AD06 IPU1_DISP1_DATA03 IPU1_CSI1_DATA03 SRC_BOOT_CFG06 EPDC_SDCE2	GPIO3[6]	
191	3V3	EIM_DA7	EIM_DA7	EIM_AD07 IPU1_DISP1_DATA02 IPU1_CSI1_DATA02 SRC_BOOT_CFG07 EPDC_SDCE3	GPIO3[7]	
192	3V3	EIM_DA8	EIM_DA8	EIM_AD08 IPU1_DISP1_DATA01 IPU1_CSI1_DATA01 SRC_BOOT_CFG08 EPDC_SDCE4	GPIO3[8]	
193	3V3	EIM_DA9	EIM_DA9	EIM_AD09 IPU1_DISP1_DATA00 IPU1_CSI1_DATA00 SRC_BOOT_CFG09 EPDC_SDCE5	GPIO3[9]	
194	3V3	EIM_DA10	EIM_DA10	EIM_AD10 IPU1_DI1_PIN15 IPU1_CSI1_DATA_EN SRC_BOOT_CFG10 EPDC_DATA01	GPIO3[10]	
195	3V3	EIM_DA11	EIM_DA11	EIM_AD11 IPU1_DI1_PIN02 IPU1_CSI1_HSYNC SRC_BOOT_CFG11 EPDC_DATA03	GPIO3[11]	
196	3V3	EIM_DA12	EIM_DA12	EIM_AD12 IPU1_DI1_PIN03 IPU1_CSI1_VSYNC SRC_BOOT_CFG12 EPDC_DATA02	GPIO3[12]	
197	3V3	EIM_DA13	EIM_DA13	EIM_AD13 IPU1_DI1_D0_CS SRC_BOOT_CFG13 EPDC_DATA13	GPIO3[13]	
198	3V3	EIM_DA14	EIM_DA14	EIM_AD14 IPU1_DI1_D1_CS SRC_BOOT_CFG14 EPDC_DATA14	GPIO3[14]	
199	3V3	EIM_DA15	EIM_DA15	EIM_AD15 IPU1_DI1_PIN01 IPU1_DI1_PIN04 SRC_BOOT_CFG15 EPDC_DATA09	GPIO3[15]	
200	GND	GND				