

PIN	Type	Function	i.MX53 Pad Name	Alternate functions	GPIO	Description (refer to i.MX53 manuals for details)
108	3V3	CSI0_DAT17	CSI0_DAT17	CSI0_D[17] UART4_CTS USBOH3_USBH3_DATA[5]	GPIO6[3]	
109	3V3	CSI0_DAT18	CSI0_DAT18	CSI0_D[18] UART5_RTS USBOH3_USBH3_DATA[6]	GPIO6[4]	
110	3V3	CSI0_DAT19	CSI0_DAT19	CSI0_D[19] UART5_CTS USBOH3_USBH3_DATA[7] USBPHY2_BISTOK	GPIO6[5]	
111	GND	GND				
112	3V3	CSI0_HSYNC	CSI0_MCLK	CSI0_HSYNC CCM_CSI0_MCLK	GPIO5[19]	
113	3V3	CSI0_VSYNC	CSI0_VSYNC	CSI0_VSYNC	GPIO5[21]	
114	3V3	CSI0_PIXCLK	CSI0_PIXCLK	CSI0_PIXCLK	GPIO5[18]	
115	3V3	CSI0_MCLK	GPIO_0	CCM_CLKO KPP_COL[5] CCM_SSI_EXT1_CLK EPIT1_EPITO SRTC_ALARM_DEB USBOH3_USBH1_PWR TD	GPIO1[0]	
116	GND	GND				

LCD Controller and Smart LCD Controller

117	3V0	LD0	DISP0_DAT0	DISP0_DAT[0] CSPI_SCLK USBOH3_USBH2_DATA[0] USBPHY2_TXREADY	GPIO4[21]	TX53 standard version: LCD Data Bus
	LVDS		LVDS1_TX2_N	not available		TX53 LVDS version: LVDS display output port 1
118	3V0	LD1	DISP0_DAT1	DISP0_DAT[1] CSPI_MOSI USBOH3_USBH2_DATA[1] USBPHY2_RXVALID	GPIO4[22]	TX53 standard version: LCD Data Bus
	LVDS		LVDS1_TX1_N	not available		TX53 LVDS version: LVDS display output port 1
119	3V0	LD2	DISP0_DAT2	DISP0_DAT[2] CSPI_MISO USBOH3_USBH2_DATA[2] USBPHY2_RXACTIVE	GPIO4[23]	TX53 standard version: LCD Data Bus
	LVDS		LVDS1_TX2_P	not available		TX53 LVDS version: LVDS display output port 1
120	3V0	LD3	DISP0_DAT3	DISP0_DAT[3] CSPI_SS0 USBOH3_USBH2_DATA[3] USBPHY2_RXERROR	GPIO4[24]	TX53 standard version: LCD Data Bus
	LVDS		LVDS1_TX1_P	not available		TX53 LVDS version: LVDS display output port 1
121	3V0	LD4	DISP0_DAT4	DISP0_DAT[4] CSPI_SS1 USBOH3_USBH2_DATA[4] USBPHY2_SIECLOCK	GPIO4[25]	TX53 standard version: LCD Data Bus
	LVDS		LVDS1_TX3_N	not available		TX53 LVDS version: LVDS display output port 1
122	3V0	LD5	DISP0_DAT5	DISP0_DAT[5] CSPI_SS2 USBOH3_USBH2_DATA[5] USBPHY2_LINESTATE[0]	GPIO4[26]	TX53 standard version: LCD Data Bus
	LVDS		LVDS1_TX0_N	not available		TX53 LVDS version: LVDS display output port 1
123	3V0	LD6	DISP0_DAT6	DISP0_DAT[6] CSPI_SS3 USBOH3_USBH2_DATA[6] USBPHY2_LINESTATE[1]	GPIO4[27]	TX53 standard version: LCD Data Bus
	LVDS		LVDS1_TX3_P	not available		TX53 LVDS version: LVDS display output port 1
124	3V0	LD7	DISP0_DAT7	DISP0_DAT[7] CSPI_RDY USBOH3_USBH2_DATA[7] USBPHY2_VBUSVALID	GPIO4[28]	TX53 standard version: LCD Data Bus
	LVDS		LVDS1_TX0_P	not available		TX53 LVDS version: LVDS display output port 1
125	3V0	LD8	DISP0_DAT8	DISP0_DAT[8] PWM1_PWMO WDOG1_WDOG_B USBPHY2_AVALID	GPIO4[29]	TX53 standard version: LCD Data Bus
	LVDS		LVDS1_CLK_N	not available		TX53 LVDS version: LVDS display output port 1

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126	3V0	LD9	DISP0_DAT9	DISP0_DAT[9] PWM2_PWMO WDOG2_WDOG_B USBPHY2_VSTATUS[0]	GPIO4[30]	TX53 standard version: LCD Data Bus
	LVDS		LVDS0_TX3_P	not available		TX53 LVDS version: LVDS display output port 0
127	3V0	LD10	DISP0_DAT10	DISP0_DAT[10] USBOH3_USBH2_STP USBPHY2_VSTATUS[1]	GPIO4[31]	TX53 standard version: LCD Data Bus
	LVDS		LVDS1_CLK_P	not available		TX53 LVDS version: LVDS display output port 1
128	3V0	LD11	DISP0_DAT11	DISP0_DAT[11] USBOH3_USBH2_NXT USBPHY2_VSTATUS[2]	GPIO5[5]	TX53 standard version: LCD Data Bus
	LVDS		LVDS0_TX3_N	not available		TX53 LVDS version: LVDS display output port 0
129	GND	GND				
130	3V0	LD12	DISP0_DAT12	DISP0_DAT[12] USBOH3_USBH2_CLK USBPHY2_VSTATUS[3]	GPIO5[6]	TX53 standard version: LCD Data Bus
	LVDS		LVDS0_CLK_P	not available		TX53 LVDS version: LVDS display output port 0
131	3V0	LD13	DISP0_DAT13	DISP0_DAT[13] AUD5_RXFS USBPHY2_VSTATUS[4]	GPIO5[7]	TX53 standard version: LCD Data Bus
	LVDS		LVDS0_TX2_P	not available		TX53 LVDS version: LVDS display output port 0
132	3V0	LD14	DISP0_DAT14	DISP0_DAT[14] AUD5_RXC USBPHY2_VSTATUS[5]	GPIO5[8]	TX53 standard version: LCD Data Bus
	LVDS		LVDS0_CLK_N	not available		TX53 LVDS version: LVDS display output port 0
133	3V0	LD15	DISP0_DAT15	DISP0_DAT[15] ECSPI1_SS1 ECSPI2_SS1 USBPHY2_VSTATUS[6]	GPIO5[9]	TX53 standard version: LCD Data Bus
	LVDS		LVDS0_TX2_N	not available		TX53 LVDS version: LVDS display output port 0
134	3V0	LD16	DISP0_DAT16	DISP0_DAT[16] ECSPI2_MOSI AUD5_TXC SDMA_EXT_EVENT[0] USBPHY2_VSTATUS[7]	GPIO5[10]	TX53 standard version: LCD Data Bus
	LVDS		LVDS0_TX1_P	not available		TX53 LVDS version: LVDS display output port 0
135	3V0	LD17	DISP0_DAT17	DISP0_DAT[17] ECSPI2_MISO AUD5_TXD SDMA_EXT_EVENT[1]	GPIO5[11]	TX53 standard version: LCD Data Bus
	LVDS		LVDS0_TX0_P	not available		TX53 LVDS version: LVDS display output port 0
136	3V0	LD18	DISP0_DAT18	DISP0_DAT[18] ECSPI2_SS0 AUD5_TXFS AUD4_RXFS WEIM_CS[2]	GPIO5[12]	TX53 standard version: LCD Data Bus
	LVDS		LVDS0_TX1_N	not available		TX53 LVDS version: LVDS display output port 0
137	3V0	LD19	DISP0_DAT19	DISP0_DAT[19] ECSPI2_SCLK AUD5_RXD AUD4_RXC WEIM_CS[3]	GPIO5[13]	TX53 standard version: LCD Data Bus
	LVDS		LVDS0_TX0_N	not available		TX53 LVDS version: LVDS display output port 0
138	3V0	LD20	DISP0_DAT20	DISP0_DAT[20] ECSPI1_SCLK AUD4_TXC	GPIO5[14]	TX53 standard version: LCD Data Bus
	SATA		SATA_RXM	not available		TX53 LVDS version: SATA port
139	3V0	LD21	DISP0_DAT21	DISP0_DAT[21] ECSPI1_MOSI AUD4_TXD	GPIO5[15]	TX53 standard version: LCD Data Bus
	SATA		SATA_TXM	not available		TX53 LVDS version: SATA port

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140	3V0	LD22	DISP0_DAT22	DISP0_DAT[22] ECSP11_MISO AUD4_TXFS	GPIO5[16]	TX53 standard version: LCD Data Bus
	SATA		SATA_RXP	not available		TX53 LVDS version: SATA port
141	3V0	LD23	DISP0_DAT23	DISP0_DAT[23] ECSP11_SS0 AUD4_RXD	GPIO5[17]	TX53 standard version: LCD Data Bus
	SATA		SATA_TXP	not available		TX53 LVDS version: SATA port
142	GND	GND				
143	3V0	HSYNC	DIO_PIN2	DIO_PIN2 AUD6_TXD USBPHY1_ENDSESSION	GPIO4[18]	
144	3V0	VSYNC	DIO_PIN3	DIO_PIN3 AUD6_TXFS USBPHY1_IDDIG	GPIO4[19]	
145	3V0	OE_ACD	DIO_PIN15	DIO_PIN15 AUD6_TXC USBPHY1_BVALID	GPIO4[17]	
146	3V0	LSCLK	DIO_DISP_CLK	DIO_DISP_CLK USBOH3_USBH2_DIR USBPHY1_AVALID	GPIO4[16]	
147	GND	GND				

Module Specific Signals

148	3V3	CSI1_MCLK	NANDF_CS2	NANDF_CS[2] SISG[0] / ESAI1_TX0 WEIM_CRE CCM_CSIO_MCLK MLBSIG USBPHY1_VSTATUS[6]	GPIO6[15]	
149	3V3	CSI1_PIXCLK	EIM_A16	WEIM_A[16] DI1_DISP_CLK CSI1_PIXCLK BT_CFG1[1]	GPIO2[22]	
150	3V3	CSI1_VSYNC	EIM_D29	WEIM_D[29] UART2_RTS DISPB0_SER_RS CSPI_SS0 / DI1_PIN15 CSI1_VSYNC DIO_PIN14	GPIO3[29]	
151	3V3	CSI1_HSYNC	EIM_EB3	WEIM_EB[3] UART3_RTS UART1_RI / DI1_PIN3 CSI1_HSYNC DI1_PIN16	GPIO2[31]	
152	3V3	CSI1_D[12]	EIM_A17	WEIM_A[17] DISP1_DAT[12] CSI1_D[12] BT_CFG1[2]	GPIO2[21]	
153	3V3	CSI1_D[13]	EIM_A18	WEIM_A[18] DISP1_DAT[13] CSI1_D[13] BT_CFG1[3]	GPIO2[20]	
154	3V3	CSI1_D[14]	EIM_A19	WEIM_A[19] DISP1_DAT[14] CSI1_D[14] BT_CFG1[4]	GPIO2[19]	
155	3V3	CSI1_D[15]	EIM_A20	WEIM_A[20] DISP1_DAT[15] CSI1_D[15] BT_CFG1[5]	GPIO2[18]	
156	3V3	CSI1_D[16]	EIM_A21	WEIM_A[21] DISP1_DAT[16] CSI1_D[16] BT_CFG1[6]	GPIO2[17]	
157	3V3	CSI1_D[17]	EIM_A22	WEIM_A[22] DISP1_DAT[17] CSI1_D[17] BT_CFG1[7]	GPIO2[16]	
158	3V3	CSI1_D[18]	EIM_A23	WEIM_A[23] DISP1_DAT[18] CSI1_D[18] / SISG[3] USBPHY2_ENDSESSION	GPIO6[6]	
159	3V3	CSI1_D[19]	EIM_A24	WEIM_A[24] DISP1_DAT[19] CSI1_D[19] / SISG[2] USBPHY2_BVALID	GPIO5[4]	

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160	GND	GND				
161	3V3		CSI0_DAT8	CSI0_D[8] / KPP_COL[7] ECSPI2_SCLK USBOH3_USBH3_OC I2C1_SDA	GPIO5[26]	
162	3V3		CSI0_DAT9	CSI0_D[9] / KPP_ROW[7] ECSPI2_MOSI USBOH3_USBH3_PWR I2C1_SCL	GPIO5[27]	
163	3V3		CSI0_DAT10	CSI0_D[10] UART1_TXD ECSPI2_MISO AUD3_RXC	GPIO5[28]	
164	3V3		CSI0_DAT11	CSI0_D[11] UART1_RXD ECSPI2_SS0 AUD3_RXFS	GPIO5[29]	
165	3V3		EIM_D22	WEIM_D[22] DIO_PIN1 DISPB0_SER_DIN CSPI_MISO USBOH3_USBOTG_PWR	GPIO3[22]	
166	3V3		EIM_D23	WEIM_D[23] UART3_CTS UART1_DCD DIO_D0_CS DI1_PIN2 CSI1_DATA_EN DI1_PIN14	GPIO3[23]	
167	3V3	CKIH1	CKIH1			
168	3V3	TVDAC_IOB	TVDAC_IOB			
169	3V3	TVDAC_IQG	TVDAC_IQG			
170	3V3	TVDAC_IOR	TVDAC_IOR			
171	GND	GND				
172	2V8		GPIO_13		GPIO4[3]	Not available on TX53 version v2
173	3V3	EIM_CS0	EIM_CS0	WEIM_CS[0] ECSPI2_SCLK DI1_PIN5	GPIO2[23]	
174	3V3	EIM_CS1	EIM_CS1	WEIM_CS[1] ECSPI2_MOSI DI1_PIN6	GPIO2[24]	
175	3V3	GPIO	CSI0_DATA_EN	CSI0_DATA_EN	GPIO5[20]	EIM_DTACK is used on the TX51, this function is not supported by the TX53
176	3V3	EIM_WAIT	EIM_WAIT	WEIM_WAIT WEIM_DTACK_B	GPIO5[0]	
177	3V3	EIM_EB0	EIM_EB0	WEIM_EB[0] DISP1_DAT[11] CSI1_D[11] GPC_PMIC_RDY BT_CFG2[7]	GPIO2[28]	
178	3V3	EIM_EB1	EIM_EB1	WEIM_EB[1] DISP1_DAT[10] CSI1_D[10] BT_CFG2[6]	GPIO2[29]	
179	3V3	EIM_OE	EIM_OE	WEIM_OE ECSPI2_MISO DI1_PIN7 USBPHY2_IDDIG	GPIO2[25]	
180	3V3	EIM_LBA	EIM_LBA	WEIM_LBA ECSPI2_SS1 DI1_PIN17 BT_CFG1[0]	GPIO2[27]	
181	3V3	EIM_RW	EIM_RW	WEIM_RW ECSPI2_SS0 DI1_PIN8 USBPHY2_ HOSTDISCONNECT	GPIO2[26]	
182	3V3	EIM_BCLK	EIM_BCLK	WEIM_BCLK		
183	GND	GND				
184	3V3	EIM_DA0	EIM_DA0	NAND_WEIM_DA[0]		Fixed function used for NAND flash

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185	3V3	EIM_DA1	EIM_DA1	NAND_WEIM_DA[1]		Fixed function used for NAND flash
186	3V3	EIM_DA2	EIM_DA2	NAND_WEIM_DA[2]		Fixed function used for NAND flash
187	3V3	EIM_DA3	EIM_DA3	NAND_WEIM_DA[3]		Fixed function used for NAND flash
188	3V3	EIM_DA4	EIM_DA4	NAND_WEIM_DA[4]		Fixed function used for NAND flash
189	3V3	EIM_DA5	EIM_DA5	NAND_WEIM_DA[5]		Fixed function used for NAND flash
190	3V3	EIM_DA6	EIM_DA6	NAND_WEIM_DA[6]		Fixed function used for NAND flash
191	3V3	EIM_DA7	EIM_DA7	NAND_WEIM_DA[7]		Fixed function used for NAND flash
192	3V3	EIM_DA8	EIM_DA8	NAND_WEIM_DA[8] DISP1_DAT[1] CSI1_D[1] / BT_CFG3[3]	GPIO3[8]	
193	3V3	EIM_DA9	EIM_DA9	NAND_WEIM_DA[9] DISP1_DAT[0] CSI1_D[0] / BT_CFG3[2]	GPIO3[9]	
194	3V3	EIM_DA10	EIM_DA10	NAND_WEIM_DA[10] DI1_PIN15 CSI1_DATA_EN BT_CFG3[1]	GPIO3[10]	
195	3V3	EIM_DA11	EIM_DA11	NAND_WEIM_DA[11] DI1_PIN2 / CSI1_HSYNC	GPIO3[11]	
196	3V3	EIM_DA12	EIM_DA12	NAND_WEIM_DA[12] DI1_PIN3 CSI1_VSYNC	GPIO3[12]	
197	3V3	EIM_DA13	EIM_DA13	NAND_WEIM_DA[13] DI1_D0_CS CCM_DI1_EXT_CLK	GPIO3[13]	
198	3V3	EIM_DA14	EIM_DA14	NAND_WEIM_DA[14] DI1_D1_CS CCM_DI0_EXT_CLK	GPIO3[14]	
199	3V3	EIM_DA15	EIM_DA15	NAND_WEIM_DA[15] DI1_PIN1 DI1_PIN4	GPIO3[15]	
200	GND	GND				